

Contact and Etching

Impact of Material Defects on SiC Schottky Barrier Diodes

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Electrical Properties and Interface Reaction of Annealed Cu/4H-SiC Schottky Rectifiers

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Microstructural Interpretation of Ni Ohmic Contact on n-type 4H-SiC

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Reduction of the Barrier Height and Enhancement of Tunneling Current on Titanium Contacts Using Embedded Au Nano-particles on 4H- and 6H-Silicon Carbide

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A Study on the Reactive Ion Etching of SiC Single Crystals Using Inductively Coupled Plasma of NF₃ –based Gas Mixtures

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Photoelectrochemical Etching Process of 6H-SiC Wafers Using HF-based Solution and H₂O₂ Solution as Electrolytes

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Growth of SiC on Si(100) by LPCVD and Patterning of the Grown Layers

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This paper describes a study on the effect of material defects on SiC Schottky barrier diodes (SBDs). Similar experiments on SiC PN diodes have been reported recently [1, 2]. In this study we construct a detailed map of defects on a test wafer using SWBXT and EBIC, observe the electrical behavior of small diodes that are either defect free or contain a known defect, and determine the correlation between the observed electrical behavior and the presence of defects within the device. The study is conducted on a 50 mm diameter n-type 4H-SiC substrate with a 10 μm n-type epilayer doped $1 \times 10^{16} \text{ cm}^{-3}$ with nitrogen. Individual die 2 mm square are defined by RIE. Each wafer is then mapped using SWBXT and EBIC, and SBDs ranging in diameter from 30 – 200 μm are fabricated within each die. Edge termination is formed by implanting $1 \times 10^{15} \text{ cm}^{-2}$ boron atoms at 30 keV in 30 μm rings surrounding each diode. The implants are activated at 1050°C to remove lattice damage without activating the dopants [3]. Nickel Schottky contacts are deposited by E-beam evaporation and patterned by liftoff.

I-V measurements, shown in Figure 1, indicate a barrier height of 1.4 eV, an ideality factor of 1.1, and a typical breakdown voltage of over 1400 V. Leakage measurements on 200 devices reveal 158 diodes with nearly identical leakage characteristics, similar to those previously reported [4]. The other 42 diodes exhibit excessive reverse bias leakage, as illustrated in Figure 2.

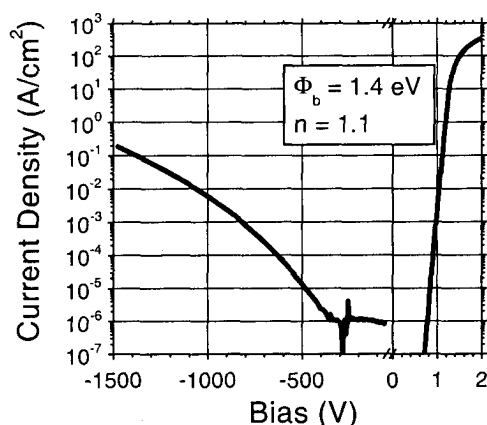


Figure 1: Forward and reverse bias I-V characteristics of nickel 4H-SiC Schottky barrier diodes

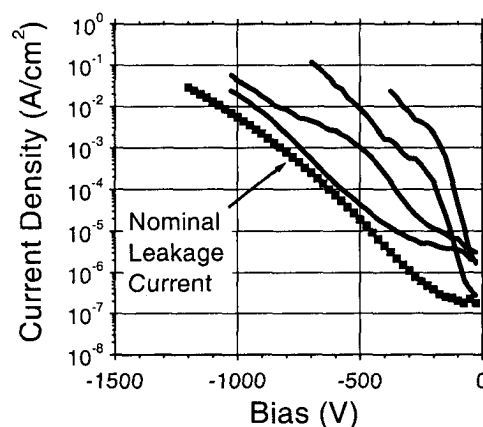


Figure 2: Comparison of reverse bias leakage current density

Examples of the obtained SWBXT and EBIC images are shown in Figure 3, including an overlay of the two images. As was demonstrated by Schnabel, *et al.* [5], each screw dislocation (SD) identified in the SWBXT images correlates to a unique recombination center (RC) visible in the corresponding EBIC image. The images are used to collect defect concentration statistics and to determine the location of each defect relative to the 200 sample diodes.

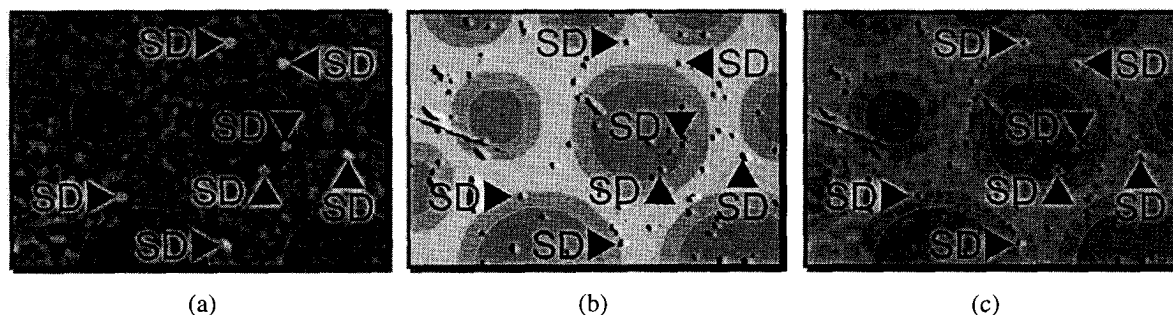


Figure 3: (a) SWBXT image, (b) EBIC image, (c) SWBXT / EBIC image overlay, indicating the location of screw dislocations (SDs) and other recombination centers (RCs) relative to several diodes.

Note that each SD corresponds to a RC, but not all RCs are due to SDs.

The average screw dislocation (SD) density identified by SWBXT is $4,096 \text{ cm}^{-2}$ and the EBIC defect density is $29,400 \text{ cm}^{-2}$. Of 200 diodes, 59% contain SD's and 98% contain EBIC defects. Diodes are classified as 1) defect free, 2) SD in diode area, 3) SD in edge termination ring, 4) EBIC defect in diode area, and 5) EBIC defect in termination ring. The collected statistics are summarized in Table 1.

	% Bad Devices with Defect	% Good Devices with Defect
Screw Dislocations	60%	58%
Active Area	19%	19%
Edge Termination	52%	51%
Boundary	26%	27%
Recombination Centers	98%	97%
Active Area	71%	61%
Edge Termination	98%	96%
Boundary	86%	75%

Table 1: Probability of finding SDs and RCs in or near diodes with good or bad leakage characteristics

Surprisingly, to within statistical error, the probability of finding a good device is the same for each category, indicating there is no correlation between SD's or EBIC defects and excessive leakage characteristics. In fact, 58% of the 158 well-behaved diodes contain SD's and 97% contain EBIC defects, while 40% of the diodes with excessive leakage current are completely free of SD's. This unexpected result suggests that, unlike SiC PN diodes [1,2], the reverse leakage current in SiC SBDs is not dominated by either SD's or EBIC defects. While these defects may impact device performance in other ways, they do not appear to prevent the manufacture of high-voltage low-leakage SiC SBDs. A more detailed discussion of these results will be presented at the conference.

Acknowledgements: We thank P. G. Neudeck and S. G. Bailey, NASA Glenn Research Center, for assistance with processing, EBIC imaging, and for helpful conversations, and M. Dudley of SUNY Stony Brook for SWBXT imaging. This work is supported by ONR/MURI grant No. N00014-95-1-1302.

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Electrical Properties and Interface Reaction of Annealed Cu/4H-SiC Schottky Rectifiers

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Nowadays, high-blocking voltage 4H-SiC Schottky rectifiers have been demonstrated. To realize stable electrical properties under high-power and high-temperature operations for a Schottky rectifier, it is important to form a reliable metal contact. Copper (Cu) is one of the expecting materials because of its low resistivity and high thermal conductivity. Our group has reported the electrical properties of Cu/6H-SiC junctions [1]. In this paper, the relation between stability of electrical properties and chemical reactions at Cu/4H-SiC Schottky interface by thermal annealing was revealed for the first time.

An n-type 4H-SiC homoepitaxial layer with a 10 μ m thick and a donor concentration of $1.0 \sim 1.4 \times 10^{16} \text{ cm}^{-3}$ grown on (0001) Si-face substrates were used. An ohmic contact on the back of substrate was employed by the deposition of nickel and annealed in N_2 ambient at 1000°C. Copper contacts were deposited by the RF sputtering method at room temperature. Diameter and thickness of copper contacts were 200 μ m and 200nm, respectively. To analyze effects of thermal annealing, an as-deposited Cu/4H-SiC junction was treated in N_2 ambient at 300~700°C for 5 minutes.

Figure 1 shows current density-voltage characteristics at room temperature for typical Cu/4H-SiC Schottky rectifiers, which had good Schottky properties. After thermal annealing at 300°C, the barrier height (ϕ_B) and ideality factor (n) was slightly increased, and the reverse leakage current could be successfully reduced. The fluctuation of electrical properties under the continuous forward bias condition is shown in Fig.2. Solid and dashed lines correspond to the as-deposited and annealed Cu/4H-SiC Schottky rectifiers, respectively. With the constant forward current at 0.125A (400A/cm²) for 1 minute, the barrier height and ideality factor of the as-deposited Cu/4H-SiC Schottky rectifier changed especially at the beginning. On the other hand, the electrical properties of annealed Cu/4H-SiC Schottky rectifiers were very stable for a long-time operation over 50 minutes. A suitable thermal annealing for a Schottky contact is very useful to improve reliability and stability in the Cu/4H-SiC electrical properties.

To discuss the electrical properties of Cu/4H-SiC Schottky contact in more detail, annealing temperature dependence of barrier height and ideality factor is studied (Fig.3). Annealing at 500°C was found to improve the Schottky barrier height, *i.e.* the barrier height increased up to about 1.75eV, and the ideality factor was kept below 1.1. The barrier height of Cu/4H-SiC could be controlled by annealing temperature. With the increase of annealing temperature over 500°C, however, Cu/4H-SiC Schottky properties became poor : Barrier heights decreased to around 1.6eV, and ideality factor increased over 1.3. Chemical bonding structures at a Cu/4H-SiC interface were analyzed by X-ray photoelectron spectroscopy (XPS) measurement, as shown in Fig.4. The reduction of Si2p binding energy and the

increase of Si2p photoelectron intensity were observed at annealing temperature over 300°C. It is considered that bonding structures of silicon atoms near the Cu/4H-SiC interface will change by the annealing, leading to the formation of stable Schottky junction and the increase of barrier height. With the increase of annealing temperature over 500°C, however, the Cu2p binding energy was increased. Copper near the interface chemically reacts with the silicon by the annealing, *i.e.* degradation of Schottky properties is caused by the formation of copper silicide at the Cu/4H-SiC interface.

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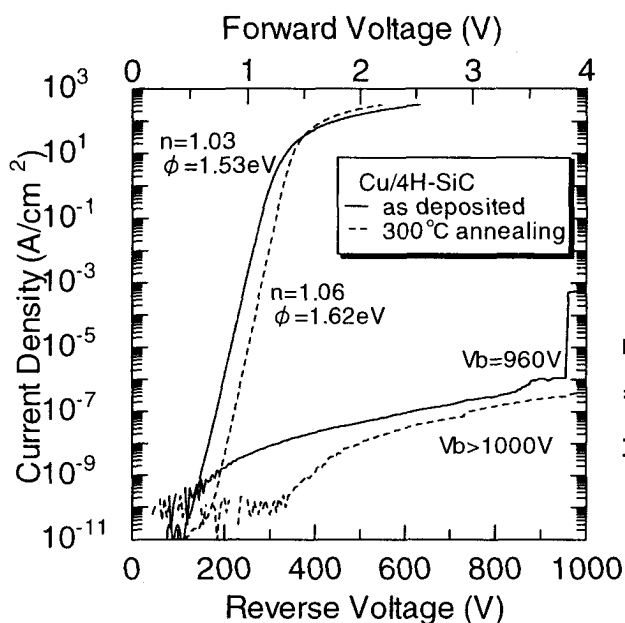


Fig.1 Current density-voltage characteristics for Cu/4H-SiC Schottky rectifiers. Solid and dashed lines correspond to as-deposited and 300°C annealed Cu contacts, respectively.

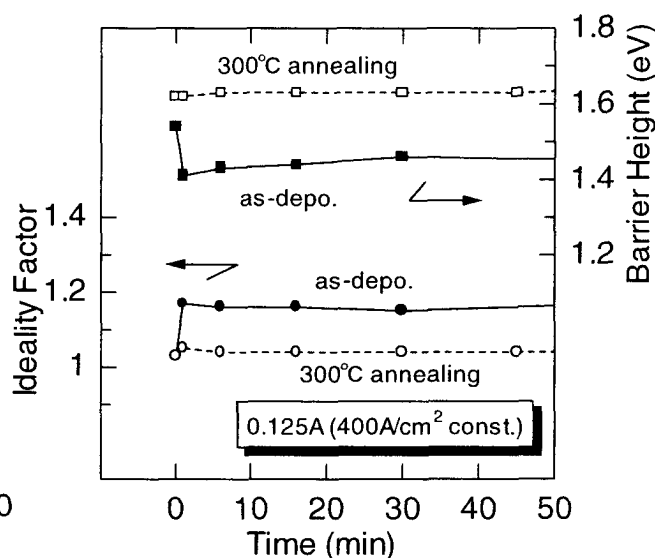


Fig.2 Operation time dependence of ideality factor and barrier height under the forward bias condition at 0.125A (400A/cm²).

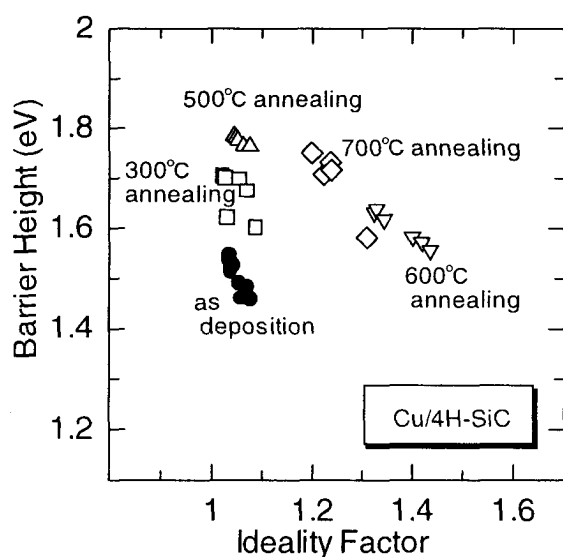


Fig.3 Annealing temperature dependence of barrier height and ideality factor for Cu/4H-SiC Schottky rectifiers.

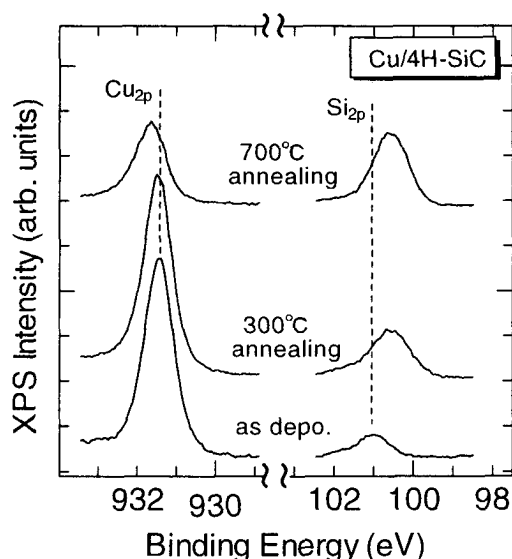


Fig.4 XPS Cu2p and Si2p core level spectra from as-deposited, 300°C, 700°C annealed Cu/4H-SiC interfaces.

Microstructural Interpretation of Ni Ohmic Contact on n-type 4H-SiC

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Ni-based metals have attracted many attentions as an ohmic contact for n-type SiC due to their low contact resistivity. The ohmic contact formation was thought to be due to the formation of Ni₂Si phase, even the Ni₂Si were formed at temperature of as low as 600 °C.¹ Thus, ohmic contact formation mechanism of Ni remains still unclear. In this work, the microstructure and electrical properties of Ni contact were studied. From these, the origin of ohmic contact formation for Ni contact on n-type SiC is proposed.

The changes for both Schottky barrier height (SBH) and ideality factor as a function of annealing temperature are shown in Fig. 1. The SBH was 1.55 eV for as-deposited Ni contact and it increased to 1.78 eV at 600 °C. When the Ni contact was annealed at 1000 °C, ohmic contact, corresponding to the SBH of 0.38 eV, was formed.

Figure 2 exhibits XRD profiles of the Ni contact with annealing temperature. After annealing at 600 °C, most of Ni film was transformed to nickel silicides composed of δ -Ni₂Si and Ni₃₁Si₁₂. After annealing at 950 °C, peaks corresponding to NiSi and graphite (002) were newly detected. These suggest that the formation of ohmic contact on n-type SiC is not due to the formation of Ni₂Si, because the ohmic contact formation temperature (>900 °C) was far from the Ni₂Si formation one (~600 °C).

Figure 3 (a) shows the XTEM micrograph of the Ni contact on n-type SiC annealed at 950 °C and, (b) and (c) show the micro diffraction patterns at the position, marked as "1" and "2", respectively. The pattern recorded near the contact, marked as "1", was indexed as NiSi and the pattern marked as "2" was indexed as δ -Ni₂Si phase, suggesting that the composition of Si in nickel silicide forming at the interface increases with annealing temperature.

The effect of elemental diffusion on the change of electrical properties was investigated by XPS with depth for Si 2p, C 1s and Ni 2p at 950 °C, shown in Fig. 4. An abundance of C atoms outdiffused through the Ni silicide and accumulated at the surface.

This suggests that the predominant outdiffusion of C atoms is closely related to the formation of ohmic contact.

In SiC, V_C act as donors for electrons and Si vacancies, V_{Si} , as acceptor. The ionization energy level of V_C is located at 0.5 eV^2 under the conduction band edge, but V_{Si} is at 0.45 eV^3 above the valence band one. A number of V_C was generated due to the outdiffusion of carbon atoms when the Ni contact was annealed at 950°C . This causes net concentration of electrons to increase under the contact because of role of V_C acting as donors. Thus, the depletion layer width and effective tunneling barrier height for the transport of electrons are simultaneously decreased, leading to the reduction of contact resistivity.

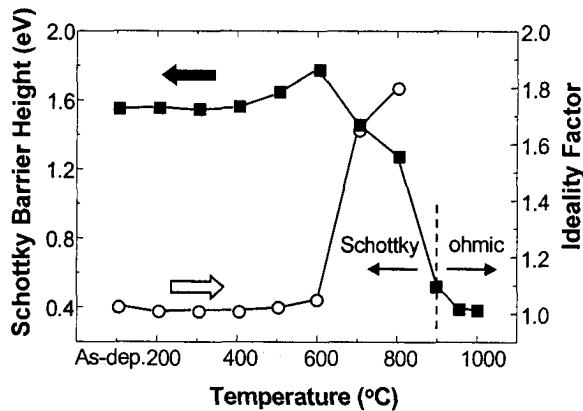


Fig. 1 Schottky barrier height and ideality factor as a function of annealing temperature

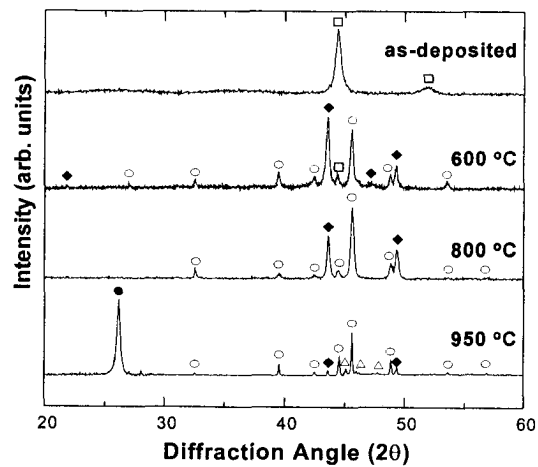


Fig. 2. Change of synchrotron X-ray diffraction pattern with annealing temperature; (□) Ni, (◆) $\text{Ni}_{31}\text{Si}_{12}$, (○) $\delta\text{-Ni}_2\text{Si}$, (△) $\eta\text{-NiSi}$, (●) graphite.

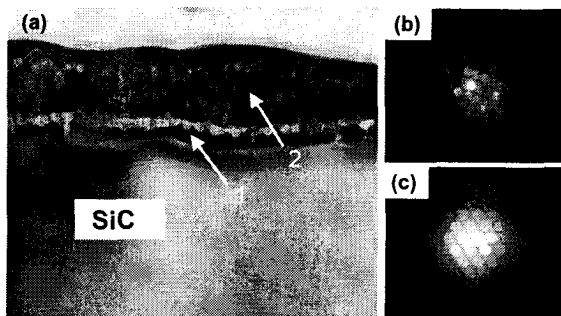


Fig. 3. (a) XTEM micrograph of Ni/SiC annealed at 950°C ; micro-diffraction patterns in areas marked (b) "1" and (c) "2".

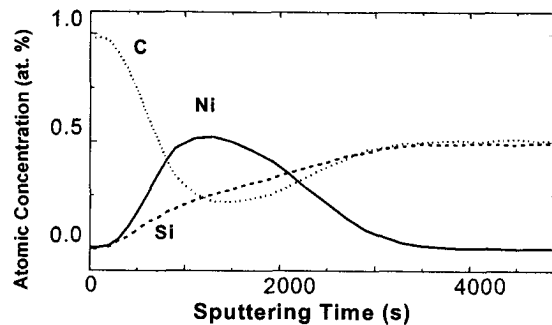


Fig. 4. XPS depth profiles of Ni, Si and C atoms for Ni contact on n-type SiC at 950°C .

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Reduction of the barrier height and enhancement of tunneling current of titanium contacts using embedded Au nano-particles on 4H- and 6H-Silicon carbide

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Ohmic contacts are difficult to achieve on SiC due to the high Schottky barrier height. For conventional Ohmic contacts, a reduction of tunneling barrier height is attained by doping the semiconductor near the surface to degenerate levels even with surface Fermi level pinning. In this work, we demonstrate a new approach for the manufacturing of Schottky contacts to n-type 4H- and 6H-SiC as well as Ohmic contacts to p-type 4H-SiC using Ti with embedded Au nano-particles on SiC based on a previous approach in a study of electron transport at the Au/InP interface [1].

The Schottky and Ohmic contacts were formed by first depositing Au aerosol particles with a diameter of 20 nm and with a density of 90~100 μm^{-2} , see Fig.1, on the SiC surface [2]. Subsequently, Ti (2000 Å) was evaporated onto the sample. The reason for selecting Au and Ti is that they have a large barrier height difference ($\Phi_{\text{bn, Au}} \approx 1.75$ eV and $\Phi_{\text{bn, Ti}} \approx 1.12$ eV). Control samples (particle-free Ti and Au, 2000 Å) were also fabricated as reference, for the Schottky contact study. Fig. 2 shows the I-V curves for Ti with embedded Au nano-particles, particle-free Ti, and Au Schottky contacts on n-type 4H-SiC as a function of the measurement temperature. From our I-V measurements, the Schottky barrier height (SBH) for Ti with embedded Au nano-particles on SiC was 0.19 eV (4H-SiC) and 0.15 eV (6H-SiC) lower than the control Ti Schottky contacts with the ideality factor of almost unity (1.04 ± 0.03 , 4H-SiC and 1.20 ± 0.13 , 6H-SiC) in the temperature range of 25-300°C. It is also clear that thermionic emission is dominant.

In order to understand this reduction of the

SBH for Ti with embedded Au nano-particles Schottky contacts to SiC, it has been proposed that SBH lowering is caused by an enhanced electric field due to the small size of the Au nano-particles and the large SBH difference. According to Tung's dipole-layer approach of the potential and the electronic transport at metal-semiconductor interfaces, the potential distribution for circular patch geometry at MS (metal-semiconductor) interfaces is given by [3]

$$V(0,0,z) = V_{bi} \left(1 - \frac{z}{W} \right)^2 + V_a + V_n - \Delta\phi_{\text{Ti-Au}} \left(1 - \frac{z}{(z^2 + R_0^2)^{1/2}} \right) \quad (1)$$

Eq. (1) suggests that the electric field at the MS interface depends on the size of the nano-particle (R_0) and SBH difference ($\Delta\phi_{\text{Ti-Au}}$) between Ti and Au metals. According to the Eq. (1), the conduction band potential for Ti embedded Au nano-particles on n-type SiC shows there is no pinch-off, indicating no electrical shielding of Au nano-particles. In forward bias, the small barrier height Ti Schottky contact conducts current dominantly for Ti with embedded Au nano-particles as shown in Fig. 2. Due to the small size of the nano-particles and large difference of SBH, the electric field is increased at the interface. As a result, the image force lowering effect of the SBH would be more significant than usual (up to ≈ 0.10 eV if $E \approx 0.068 \times 10^7$ V/cm, see Fig. 3). Other authors have simulated even higher fields, $\approx 3 \times 10^7$ V/cm in Si [4]. This theoretical calculation is in reasonable agreement with our experimental results (0.19, 0.15 eV for 4H- and 6H-SiC, respectively). However, an extended study is needed for a more solid explanation.

We have also tested these contacts on highly doped p-type SiC material. As shown in Fig. 4, the total resistance between two TLM pads (transfer length method), spaced 5 μm apart shows that Ti with embedded Au has a lower contact resistance than that of control Ti Ohmic contacts on p-type 4H-SiC. Similarly, we also explain the reduction of the Ohmic contact resistance by the enhancement of the electric field at the MS interface, which makes the SBH thinner. This has only been shown previously on silicon [4].

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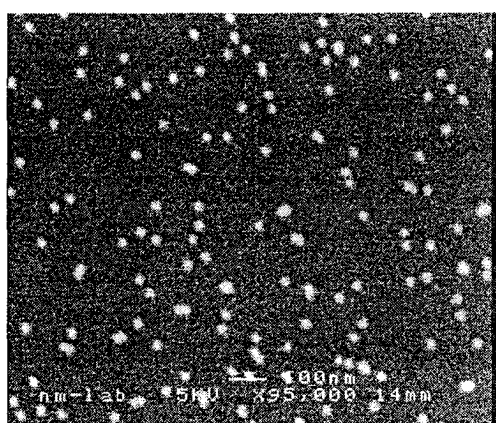


Fig. 1 SEM view of Au nano-particles (20 nm in diameter, 90 μm^{-2} in density).

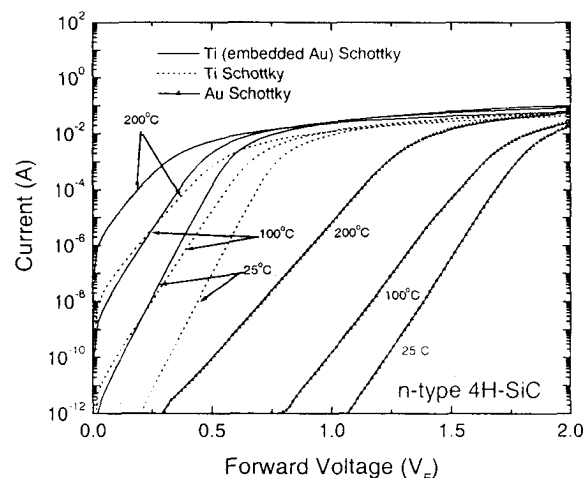


Fig. 2 I-V characteristics of Ti with embedded Au, particle-free Ti, and Au Schottky diodes to n-type 4H-SiC as a function of the measurement temperature.

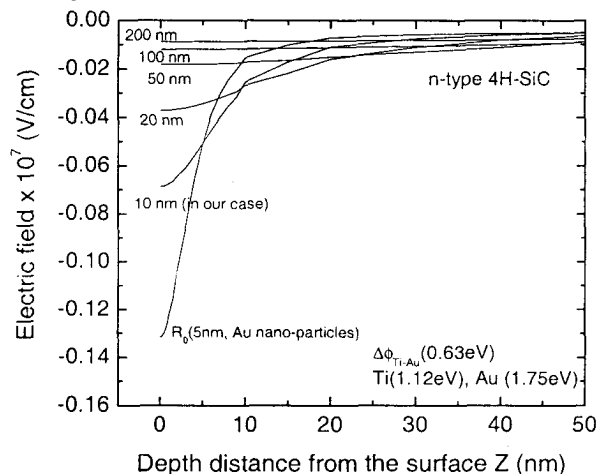


Fig. 3 Calculated electric field distribution at the MS interface using a dipole-layer approach for Ti with embedded Au Schottky diode and different radius of Au nano-particles.

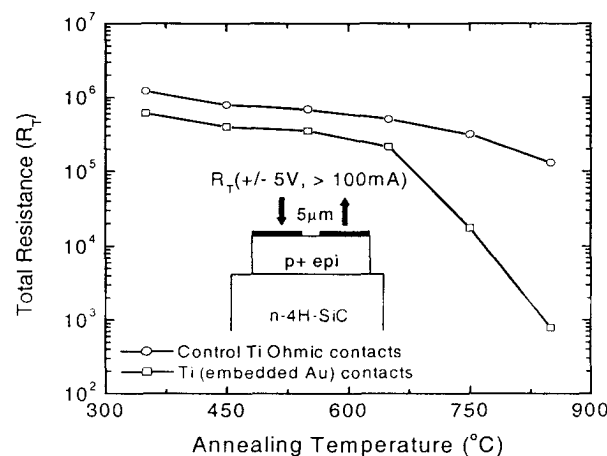


Fig. 4 Comparison of the total resistance between Ti with embedded Au and particle-free Ti Ohmic contacts to highly doped p-type 4H-SiC.

A study on the reactive ion etching of SiC single crystals using inductively coupled plasma of NF₃-based gas mixtures

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The inductively coupled plasma reactive ion etching (ICP-RIE) of SiC single crystals using the NF₃ gas mixture was investigated. Mesa profiles were studied as a function of substrate bias power (25~100W), ICP coil power (700~1000W), chamber pressure (4~10mtorr), percentages of O₂ (0~40%), and the distance between the substrate holder and the source coil.

Figure 1 shows ICP-RIE characteristics of 4H-SiC mesas as a function of various process parameters. It is observed that the etch rate increases as the ICP power (Fig 1a) and the bias power increase (Fig 1b). The etch rate decreases as the sample-coil distance (Fig 1e), O₂ % (Fig 1c), and pressure (Fig 1d) are increased. Smooth surfaces (roughness \leq ~1.5nm) and vertical sidewalls (about 85°) were maintained throughout the experiments.

Mesas with vertical sidewalls and smooth surfaces were obtained at the low bias conditions (Fig 2a), with the etch rate of up to 300nm/min, roughness of about 1nm, and verticality 85°. Higher etch rates could be obtained in the case of high bias conditions (>~300V), although severe mask damage was observed (Fig. 2b).

Investigation on the effects of addition of various gases to the NF₃ mixture on the mesa profile is in progress and the results will be discussed during the presentation. This work was performed as a part of the SiC Device Development Program (SICDDP) supported by the MOCIE (Ministry of Commerce, Industry and Energy), Korea.

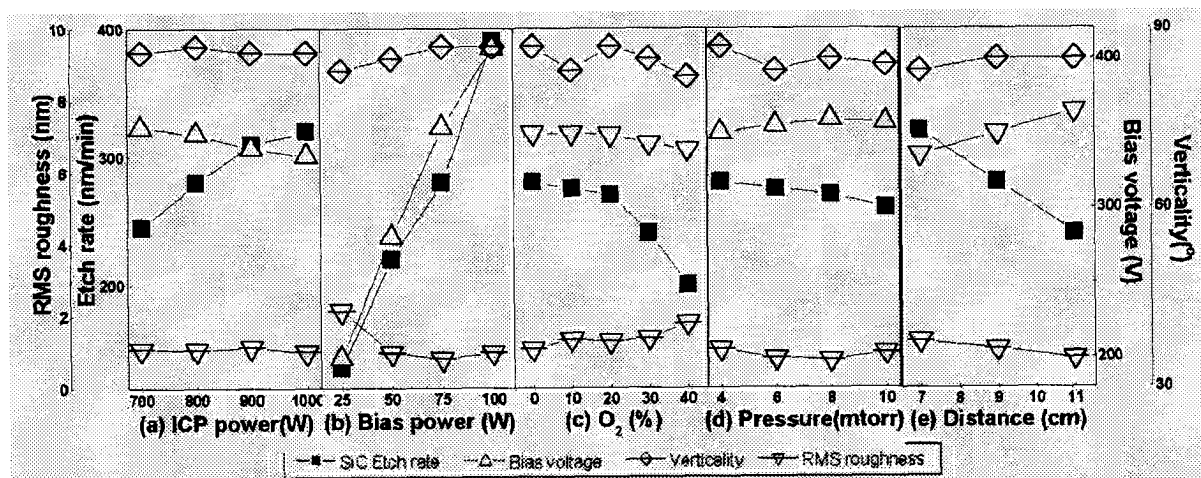


Fig. 1. Etch characteristics of 4H-SiC as a function of (a) ICP source power, (b) bias power, (c) O₂ % within NF₃-based gas, (d) pressure, and (e) sample-coil distance

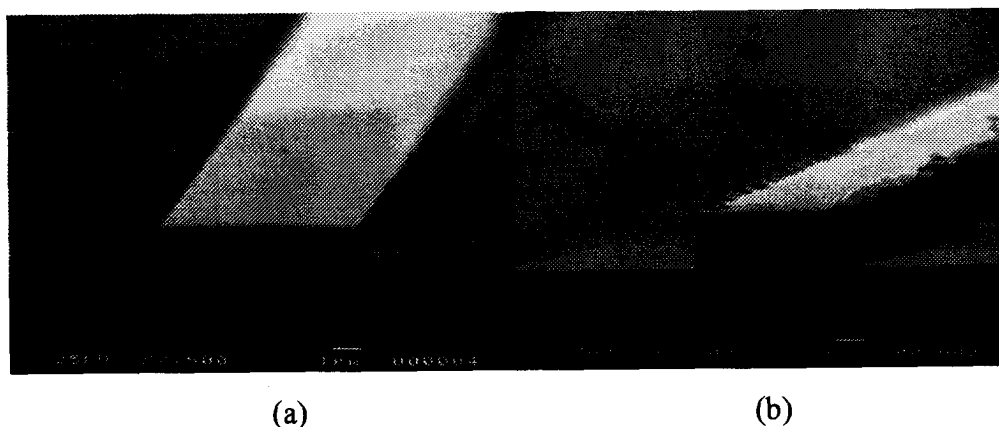


Fig. 2. Cross-sectional SEM micrographs of the SiC mesas etched at the conditions of (a) 800W_50W(280V)_4mTorr_9cm-10 min and (b) 900W_100W(410V)_4mTorr_Ar30%-3cm-10min,

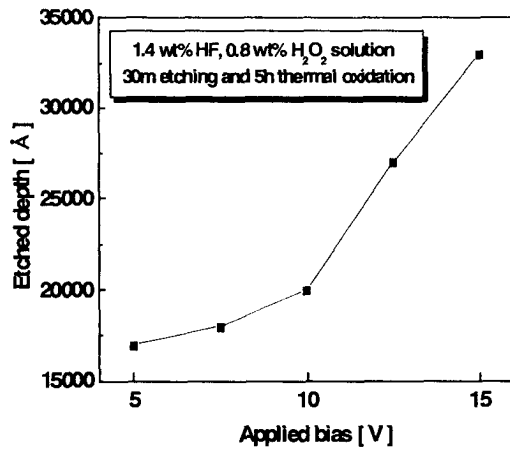
Photoelectrochemical Etching Process of 6H-SiC wafers Using HF-based Solution and H₂O₂ Solution as Electrolytes

Jung Gyun Song and Moo Whan Shin

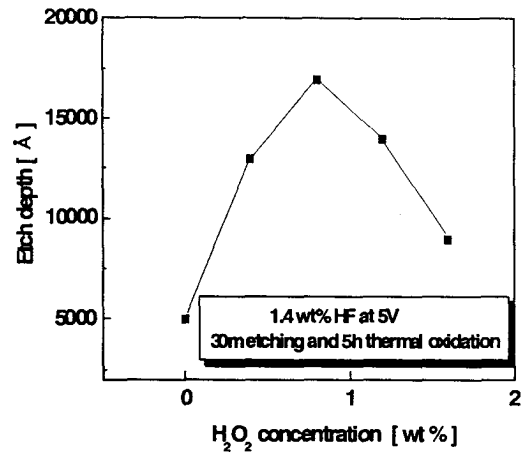
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Dry etching methods which are commonly used for the fabrication of SiC devices are known to result in ion-induced damage on the etched surface, which is highly undesirable for the high frequency and high power device operation. In this paper, we report on the photoelectrochemical (PEC) wet etching process of 6H-SiC using several electrolytes including HF-based solution, H₂O₂ solution and a mixture of HF and H₂O₂. The etching process using the HF-based solution consists of formation of porous layer on the surface of sample and thermal oxidation followed by HF dipping process to eliminate the porous layers. It is believed that the high density of pores was resulted from the reaction between oxygen and carbon. It was confirmed from the EDS analysis that most of carbon atoms were eliminated from the surface of SiC after the PEC etching, which indicates that the surface carbon was used for the formation of CO₂ or CO. An etching rate of 760 Å/min was obtained using a dilute HF (1.4 wt % in H₂O) electrolyte with the etching potential of 3.5 V. When H₂O₂ was employed as an electrolyte, an oxide layer was formed on the surface of the sample without a formation of porous layer. The formation of the oxide layer was almost linearly increased with the etching time. The thickness of oxide is about 11500 Å for the etching time of 90 min. (H₂O₂ : H₂O = 1: 210, without HF, applied bias = 2 V). The etching rate and the surface roughness were changed with the variation of etching potential and the amount of H₂O₂ into the HF electrolyte. The etching rate is increased with the applied bias in a range between 5 V and 15 V for an electrolyte with 1.4 wt % of HF and 0.8 wt % of H₂O₂ (Figure 1(a)). The etching rate is shown to be increased as the concentration of H₂O₂ is increased, but to be decreased after the concentration exceeds 0.8 wt %. The surface roughness was significantly improved when the sample was etched using the H₂O₂ without any HF in the electrolyte ; RMS roughness of about 200 Å when etched in the electrolyte with HF and 27 Å in the electrolyte with H₂O₂ only (Figure 2).

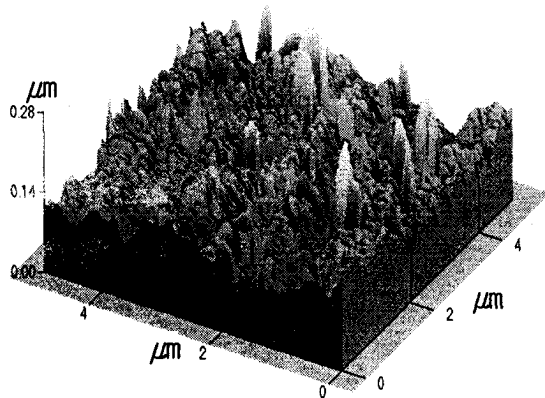


(a)

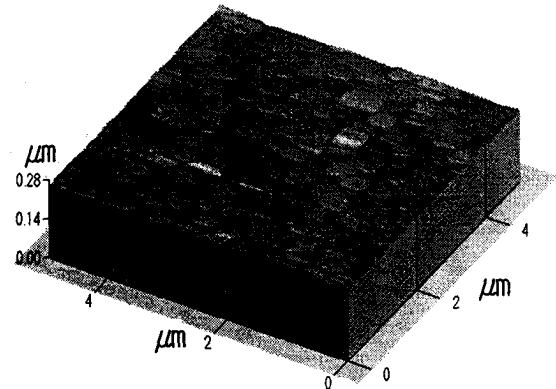


(b)

Fig. 1 Effect of applied etching potential on the etching depth for an electrolyte mixed with HF (1.4 wt %) and H₂O₂ (0.8 wt %) depth (a) and the effect of the concentration of H₂O₂ on the etching depth (etching potential of 5 V).



(a)



(b)

Fig. 2 AFM of surfaces of samples after PEC etching using ; (a) HF-based solution as an electrolyte and (b) H₂O₂ as an electrolyte. The RMS roughness of the samples are 200 Å (a) and 27 Å (b), respectively.

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Growth of SiC on Si(100) by LPCVD and Patterning of the Grown Layers

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Cubic silicon carbide (3C-SiC) is at present a topic of considerable interest due to its great promise as a material for electronic device applications and microelectromechanical systems (MEMS) in harsh environments, or for biomedical applications [1-5]. Semiconductor materials grown directly on silicon profit by the availability of low-cost large area substrates, their superior thermal conductivity and the possibility to realize a new generation of devices monolithically integrated with silicon microelectronics. Large lattice mismatch and the difference in thermal expansion coefficients cause high residual stress and substrate bending. The stress cannot be completely relaxed by the formation of misfit dislocations. It is important to employ lower growth temperatures in order to improve the quality of the heterostructure and to improve further processing. SiC replaces silicon in MEMS devices and gas-sensors for harsh environments. Due to its high chemical stability which is an advantage of silicon carbide as a material for harsh environments it is difficult to employ standard patterning approaches – wet and even dry (poor mask selectivity) etching. New growth and patterning approaches must be developed to sustain flexibility of the device design. A novel alternative processing approach to bulk micromachining of polycrystalline SiC using Si molds was recently reported [6]. The aim of the present paper is to investigate low-temperature low-pressure CVD growth of SiC on Si(100) and Si(100) with a patterned SiO₂ mask layer for patterning the grown layer without etching SiC itself.

The growth was performed in a standard horizontal infrared-heated LPCVD machine AIX-200 designed by AIXTRON and operated at low pressure (20 to 100 hPa) utilizing the precursors carbon tetrabromide (CBr₄) and monosilane (SiH₄, 2% in H₂) as sources of C and Si, respectively. For more stable operation at high temperatures the heating system has been modified. A 150 W mercury-xenon lamp as a UV-source has been added to the set-up [7]. The growth rate at 940°C was about 0.25 µm/h. Exactly (100) oriented Si substrates with or without patterned SiO₂ mask layer were employed. Our samples were grown with or without UV stimulation. Experiments with varied CBr₄/SiH₄ flow ratios were carried out. A short Si substrate-carbonisation step [1] was added in the experiments at the beginning of the SiC growth process.

The samples obtained were investigated by atomic-force microscopy (AFM), scanning electron microscopy (SEM), photoluminescence (PL), optical microscopy, transmission electron microscopy (TEM) and load-deflection measurements. In this work we concentrated our attention to the fabrication of patterned SiC on Si substrate. The UV stimulation increased the uniformity of the grown surfaces and in most cases decreased their roughness [7].

Optical microscopy and SEM investigations showed mirror-like surfaces of the grown layers. TEM investigations of these samples revealed the transition from amorphous to fine polycrystalline and then to textured 3C-SiC films with variation of the Si/C ratio in the gas phase. We found broad PL peaks around 2.4 eV with FWHM of about 0.44 eV.

The 40-90 nm thick SiC layers were patterned employing a novel lift-off approach with SiO₂ as sacrificial layer. Silicon wafers were oxidised at 1200°C (SiO₂ thickness about 1 μm) and patterned in HF. The subsequent SiC growth was optimised for the lift-off process which was carried out in buffered HF (to lift-off SiC on SiO₂). Finally, the Si was patterned employing etching in 30% KOH using the SiC as mask. A plan-view SEM image of a micro-patterned SiC lateral resonant structure is shown in Fig. 1. The edges of the patterned structure are sharp. For structures oriented along {100} directions undercut was observed. Cracking or fracturing of the undercut layers was not observed even in the case of a very small radius of bending. The layers obtained reveal exciting mechanical stability.

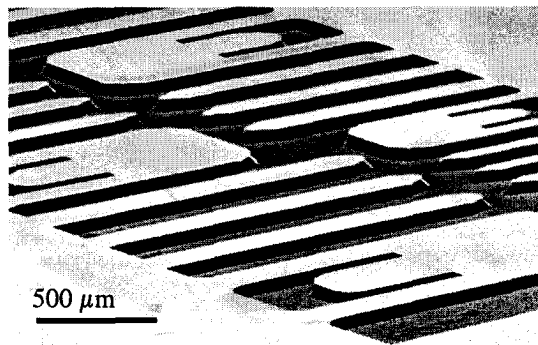


Fig. 1. Plan-view SEM image of a micro-patterned SiC lateral resonant structure grown on Si (100) substrate.

In conclusion, we have developed and described a low-cost approach to 3C-SiC LPCVD growth and patterning. LPCVD with UV stimulation has been developed as a technique for the low-temperature growth of SiC on Si with a patterned SiO₂ mask. Examples of surface micromachined structures patterned by the described lift-off approach are presented. The approach can be used for further pendeo-epitaxial growth or fabrication of micromechanical devices, gas sensors, or biomedical applications.

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